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Applicant: **Jean-Christophe Jiguet, et al.**
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Two Signals**

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PRIORITY APPLICATION UNDER 35 U.S.C. § 119**

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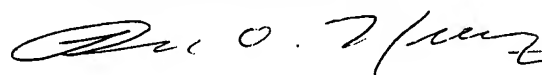
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Submitted herewith is a certified copy of the European Patent Application No. 03290003.7, filed on 01/02/2003, in the European Patent Office and from which priority under 35 U.S.C. § (e)(1) is claimed for the above-identified application.

Please charge any fees necessary to the deposit account of Texas Instruments Incorporated, Account No. 20-0668. An original and two copies of this sheet are enclosed.

Respectfully submitted,



Ronald O. Neerings
Patent Attorney
Reg. No. 34,227

Texas Instruments Incorporated
Mail Station 3999
P.O. Box 655474
Dallas, TX 75265
(972) 917-5299

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Die angehefteten Unterlagen stimmen mit der ursprünglich eingereichten Fassung der auf dem nächsten Blatt bezeichneten europäischen Patentanmeldung überein.

The attached documents are exact copies of the European patent application described on the following page, as originally filed.

Les documents fixés à cette attestation sont conformes à la version initialement déposée de la demande de brevet européen spécifiée à la page suivante.

Patentanmeldung Nr. Patent application No. Demande de brevet n°

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Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
p.o.

R C van Dijk



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Anmelder/Applicant(s)/Demandeur(s):

Texas Instruments Incorporated
7839 Churchill Way,
Mail Station 3999
Dallas,
Texas 75251
ETATS-UNIS D'AMERIQUE
TEXAS INSTRUMENTS FRANCE
B.P. 5
06270 Villeneuve Loubet
FRANCE

Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:
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Circuitry for reducing the skew between two signals

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CIRCUITRY FOR REDUCING THE SKEW BETWEEN TWO SIGNALS

BACKGROUND OF THE INVENTION

Technical Field

This invention relates in general to electronic circuits and, more particularly, to circuitry for reducing the skew between two signals.

Description Of The Related Art

In the design of electronic circuits, it is often necessary to compensate for skew between two signals arriving at a common block. Traditionally, the skew between the two signals is reduced with the addition of buffers to equalize the difference between the paths of the two signals. Often, the appropriate buffers can be determined automatically using computer aided design tools.

An example of the problem is set forth in connection with Figures 1a and 1b. Figure 1a illustrates an example a portion of an integrated circuit where signals from two different circuitry blocks (source blocks) are received at a third block (user block). First source block 10 is clocked using clock Ca and a second circuitry block 12 is clocked using clock Cb. First and second source blocks 10 and 12 could implement any type of analog or digital circuitry, or a mix thereof. As shown in Figure 1b, Clocks Ca and Cb are skewed by an amount $\text{Skew}(Ca - Cb)$. The output A of source block 10 is delayed by a time D_a due to propagation through the logic of source block 10 and routing delays between the output of source block 10 and the input to user block 14. Similarly, the output B of source block 12 is delayed by a time D_b due to propagation through the logic of source block 12 and routing delays between the output of

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source block 12 and the input to user block 14. For reference, Figure 1b is a timing diagram which shows the skew between clocks Ca and Cb at the inputs to source blocks 10 and 12, respectively, and shows the delay between the resulting signals at the input to user block 14. This delay is a factor of the skew between clocks Ca and Cb and the delays Da and Db. The delay between signals A and B at the input to user block 14 could be defined as:

$$\text{Delay}(A-B) = \text{Skew}(Ca-Cb) + Db - Da$$

In mixed signal design, there will be digital spread delays and analog spread delays. The spread of each cannot be easily compensated with a unique addition of digital delay.

Therefore a need has arisen for a method and circuit for reducing skew between two signals.

SUMMARY OF THE INVENTION

In the present invention an electronic circuit includes a first source circuit for generating a first signal and for generating a first calibration signal responsive to a calibration mode and a second source circuit of generating a second signal and for generating a second calibration signal responsive to the calibration mode. A variable delay circuit detects a delay between the first and second calibration signals and applies a delay to the first signal responsive to the detected delay.

The present invention provides significant advantages over the prior art. The variable delay circuit can provide high precision compensation for delays between two signals as determined at the input to a circuit that uses the two signals. Therefore, the variable delay circuit takes into account all sources of delay, without needing any knowledge of the sources of delay or their possible variations. Since calibration can

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occur as often as desired, the variable delay circuit can compensate for dynamically varying delays. The variable delay circuit is particularly well suited for use with analog RF designs which need frequent high precision calibration between signals.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

Figure 1a is a block diagram of an circuit illustrating the problem of skewed signals;

Figure 1b is a timing diagram for the circuit of Figure 1a;

Figure 2a is a block diagram of a prior art solution for skewed signals;

Figure 2b is a timing diagram for the prior art solution of Figure 2a;

Figure 3a is a block diagram of a circuit with a variable delay circuit to minimize delays between signals;

Figure 3b is a timing diagram for the circuit of Figure 3a; and

Figure 4 is a schematic diagram of a preferred embodiment for a variable delay circuit.

DETAILED DESCRIPTION OF THE INVENTION

The present invention is best understood in relation to Figures 1 - 4 of the drawings, like numerals being used for like elements of the various drawings.

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Figures 2a and 2b illustrate a prior art solution to the problem of signal skew. Figure 2a is the same as the example circuit of Figure 1a, with the addition of a delay buffer 16 between the output (A1) of source circuitry 10 and the input (A) to user circuitry 14. The delay D_c is calculated to compensate for the delays caused by clock skew and logic and routing delays. With the addition of delay buffer 16, the delay between signals A and B could be estimated as:

$$\text{Delay}(A-B) = \text{Skew}(C_a - C_b) + D_b - (D_a + D_c)$$

However, it should be noted that clock and signal delays are not exact, since each has a spread which may vary based on processing variations and environmental factors. Some environmental factors, such as temperature, may vary during operation of a device. Hence $C_a = C_{a_{\text{nom}}} \pm \Delta C_a$, $C_b = C_{b_{\text{nom}}} \pm \Delta C_b$, $D_a = D_{a_{\text{nom}}} \pm \Delta D_a$, $D_b = D_{b_{\text{nom}}} \pm \Delta D_b$, and $D_c = D_{c_{\text{nom}}} \pm \Delta D_c$, where "nom" indicates and expected nominal value and Δ indicates an expected variation.

In many cases, the possible variations in the delays and clock skew, along with the variation on the compensation delay, D_c , make it impossible to guarantee that the delay between the A and B signals will be within maximum design specifications.

Figures 3a and 3b illustrate a circuit using dynamic best fit delay compensation. In Figure 3a, the delay buffer 16, with fixed delay D_c , has been replaced with a variable delay buffer 18, with a dynamically variable delay component D_{cv} .

During operation of the device, a Start signal is used to calibrate the variable delay circuit 18, such that D_{cv} is set to an appropriate value that will compensate for the clock skew and delays D_a and D_b . D_{cv} is set until a reset signal initiates another calibration. Depending upon the design, the circuit

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could be calibrated upon start-up, periodically, upon an event, or upon each use of the user circuitry block 14.

Figure 4 illustrates a preferred embodiment of a variable delay buffer 18. The variable delay buffer 18 comprises a plurality of delay stages 20. A delay stage includes a fixed delay buffer 22, a flip-flop 24, an exclusive-or gate 26 and an AND gate 28. Each fixed delay buffer 22 receives the output of the fixed delay buffer of the preceding stage 20. The first stage receives the output (A1) of the first source block 10 and can optionally have a delay buffer 22 or have no delay (as shown). The output of the fixed delay buffer 22 is coupled to the input of a flip-flop 24. Flip-flop 24 is clocked by the output (B1) of the second source block 12 while the Start signal is active (in the illustrated embodiment, the Start signal is active high). The flip-flops 24 are reset by signal RESETZ (active low). The output of flip-flop 24 is coupled to the input of exclusive-or gate 26. The other input of exclusive-or gate 26 is coupled to the output of the flip-flop of the subsequent stage 20. For the last stage 20, the second input to the exclusive-or gate is tied to a logical "1". The output of exclusive-or gate 26 is coupled to one input of an AND gate 28. The other input to the AND gate is the output of the fixed buffer 22 of the same stage 20. The outputs of the AND gates of all stages are coupled to the inputs of OR gate 30. The output of the OR gate 30 is the input (A) to the user block 14.

The output (B1) of the second source block 12 is coupled to fixed delay buffer 32, with a delay D0. The output of fixed delay buffer 32 is the input to the user block 14.

In operation, the Start signal begins a calibration cycle. It is assumed that the B1 signal is known to (or is designed to) transition to an active state after the A1 signal. Prior to calibration, all flip-flops 24 are reset to output logical "0"s.

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by the RESETZ signal. When the B1 signal transitions high (active), the A1 signal will have begun propagation through the fixed delay buffers 22. When the flip-flops are set, there will be a single occurrence where flip-flops from two consecutive stages have outputs of different logical values - the earlier stage will output a logical "1" and the later stage will output a logical "0". This is the point where the active edge has propagated through the delay buffers 22.

The AND gate 28 of the stage 20 having the exclusive-or gate 26 with a "1" output will pass the output of that stage's fixed delay buffer 22. Hence, the exclusive-gates 26 and the AND gates 28 form a multiplexer which selects the output of a fixed delay buffer 22 whose cumulative delay (i.e., the delay of all buffers in the chain) most closely matches the delay between the A1 and B1 outputs. In the illustrated embodiment, the exclusive-or gates 26 are configured to choose the output of the fixed delay buffer 22 in the earlier of the two stages at which the transition occurs as the best fit delay; alternatively, the output of the fixed delay buffer 22 in the later of the two stages could be chosen as the best fit delay by coupling each exclusive-or gate to the output of the flip-flop 24 of its own stage and the output of the flip-flop 24 of the preceding stage (rather than the output of the flip-flop 24 of the subsequent stage, as shown).

Table 1 illustrates the propagation of the A1 signal through the variable delay buffer 18 during a calibration cycle. When B1 transitions to an active state, A1 has passed through the delay buffers 22 of stages 1-4, but has not yet passed through the delay buffer 22 of stage 5. If the delay of each delay buffer 22 is D, it can be said that $4 \cdot D \leq \text{Delay}(A1-B1) < 5 \cdot D$.

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TABLE 1 EXAMPLE OF VARIABLE DELAY BUFFER

Stage	Output of buffer 22	Output of flip-flop 24	Output of XOR gate 26	Output of AND gate 28
1	1	1	0	0
2	1	1	0	0
3	1	1	0	0
4	1	1	1	Output of buffer 22 of stage 4
5	0	0	0	0
6	0	0	0	0
7	0	0	0	0

The exclusive-or gate 26 for stage "4" will be the only exclusive-or gate that outputs a "1"; the remainder of the exclusive-or gates 26 will output "0"s. Accordingly, only the AND gate 28 of stage "4" will pass the output of the stage's fixed delay buffer 22. The outputs of all other AND gates 28 will be logical "0"s.

The maximum delay is provided at the output of the fixed delay buffer 22 of the last stage. If the active edge of A1 precedes the active edge of B1 by more the sum of all the fixed delay buffers 22, then the maximum delay will be used (since the input of the exclusive-or gate 26 in the last stage is set to a "1").

The implementation of the variable delay circuit 18 shown in Figure 4 is designed to minimize the delay between the A1 and B1 signals without exceeding the actual delay between the signals. Alternatively, by coupling one input of the exclusive-or gates 26 to the output of the preceding flip-flop 24, rather than the subsequent flip-flop 24, the delay provided by the variable delay circuit 18 would be the minimum delay needed to close or exceed the actual delay between the A1 and B1 signals.

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For a given maximum delay, the resolution of the variable delay circuit 18 can be increased by providing more delay elements 22, each with a smaller delay D.

After the appropriate delay buffer 22 is selected for output, the Start signal transitions to an inactive state. At this point, the appropriate delay is memorized in the variable delay circuit 18. The A1 signal will continue to pass through the chain of delay buffers 22 up to the selected delay buffer, at which point it will pass through the AND gate 28 of the associated stage and the OR gate 30 to the user block 14. This will continue until another calibration is initiated using the Start signal.

The delay buffer 32 compensates for the delays associated with the AND gate 28 and OR gate 30 through which the A1 signal must pass. However, since these delay buffer 32 is fabricated in close proximity to the AND gates 28 and OR gates 30, any variation due to processing or temperature will be closely matched.

The present invention provides significant advantages over the prior art. The variable delay circuit 18 provides high precision compensation for delays between two signals. The compensation is determined at the input to the user circuit 14 and therefore takes into account all sources of delay, without needing any knowledge of the sources of delay or their possible variations. Since calibration can occur as often as desired, the variable delay circuit 18 can compensate of dynamically varying delays. The variable delay circuit is particularly well suited for use with analog RF designs which need frequent high precision calibration between signals.

As is known to those skilled in the art, the logic used to implement the multiplexer could be varied, without changing the

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functionality of the variable delay circuit 18. The concept is easily extended to cases where the active edges of A1, B1 and Start could be logical "0"s or mixed.

Although the Detailed Description of the invention has been directed to certain exemplary embodiments, various modifications of these embodiments, as well as alternative embodiments, will be suggested to those skilled in the art. The invention encompasses any modifications or alternative embodiments that fall within the scope of the Claims.

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CLAIMS

1. An electronic circuit comprising:
 - a first source circuit for generating a first signal and for generating a first calibration signal responsive to a calibration mode;
 - a second source circuit of generating a second signal and for generating a second calibration signal responsive to the calibration mode;
 - a variable delay circuit for detecting a delay between said first and second calibration signals and applying a delay to said first signal responsive to the detected delay.
2. The electronic circuit of claim 1 and further comprising a fixed delay buffer for applying a fixed delay to said second signal to compensate for delays attributable to said variable delay circuit.
3. The electronic circuit of claim 1 or 2 wherein said variable delay circuit comprises a chain of fixed delay buffers and circuitry for selecting an output of one of said fixed delay buffers responsive to the detected delay.
4. The electronic circuit of claim 3 wherein said selecting circuitry comprises circuitry for detecting a transition of said first calibration signal in said chain of fixed delay buffers responsive to an active transition of said second calibration signal.
5. The electronic circuit of claim 4 wherein said circuitry for detecting a transition comprises a plurality of flip-flops for storing outputs of respective fixed delay buffers responsive to said active transition of said second calibration signal.

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6. An method of reducing skew between a first signal from a first source circuit and a second signal from a second source circuit, comprising the steps of:

generating a first calibration signal at the first source circuit responsive to a calibration mode;

generating a second calibration signal at the second source circuit responsive to the calibration mode;

detecting a best fit delay between said first and second calibration signals; and

passing said first signal after applying the best fit delay to said first signal.

7. The method of claim 6 and further comprising the step of applying a fixed delay to said second signal to compensate for delays attributable to said passing step.

8. The method of claim 6 or 7 wherein said detecting step comprises the steps of:

propagating the first calibration signal through a chain of fixed delay buffers; and

detecting a transition of the first calibration signal between adjacent fixed delay buffers.

9. The method of claim 8 wherein said detecting step further comprises the step of storing outputs of the fixed delay buffers in respective flip-flops.

10. The method of claim 8 wherein said passing step comprises the step of passing the output of one of said adjacent fixed delay buffers.

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CIRCUITRY FOR REDUCING THE SKEW BETWEEN TWO SIGNALS

ABSTRACT

An electronic integrated circuit includes a first signal (A1) generated by a first source block (10) and a second signal (B1) generated by a second source block (12). A variable delay circuit (18) detects a delay between said first and second signals in calibration mode and applies the delay to the first signal during normal operation of the circuit. A fixed delay buffer (32) may be used to apply a delay to the second signal to compensate for known delays associated with the variable delay circuit (18).

Figure 3a

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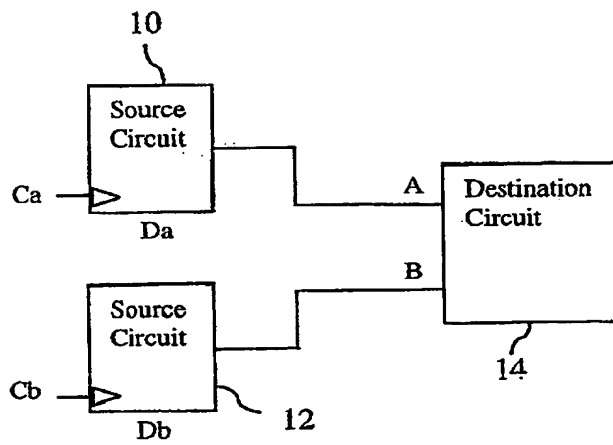


Fig. 1a

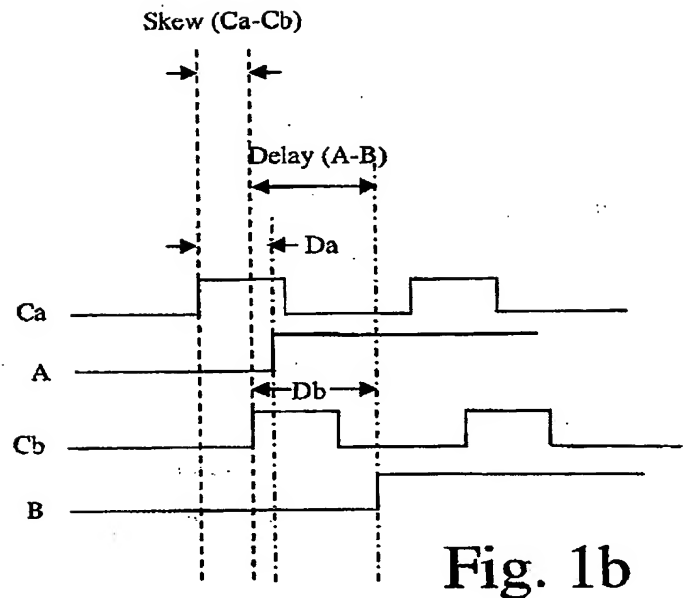


Fig. 1b

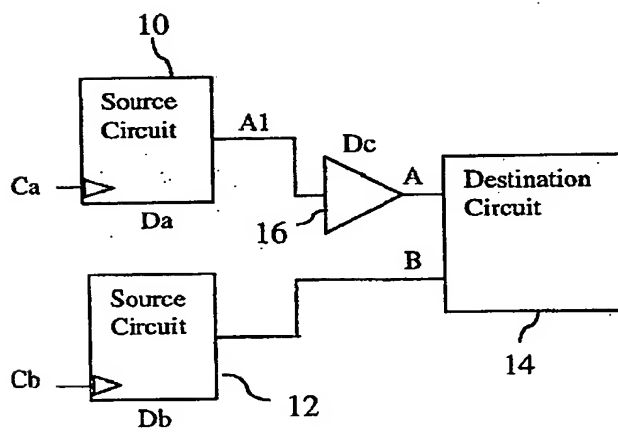


Fig. 2a
(Prior Art)

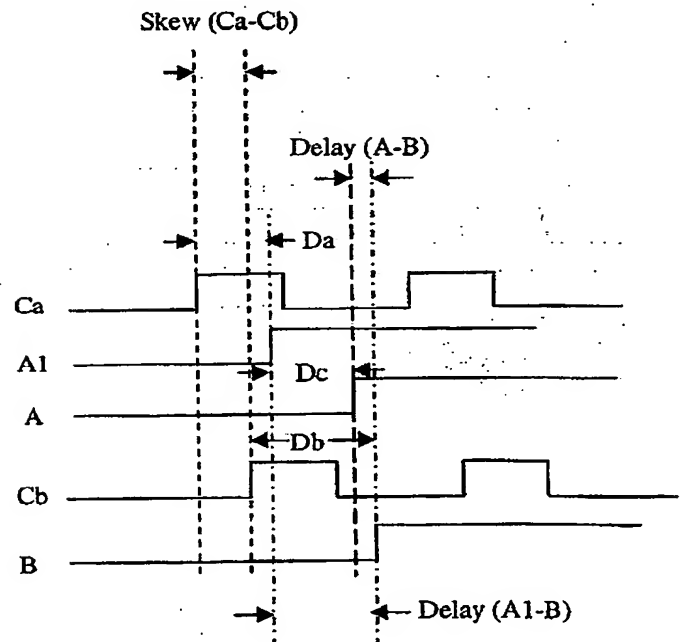


Fig. 2b
(Prior Art)

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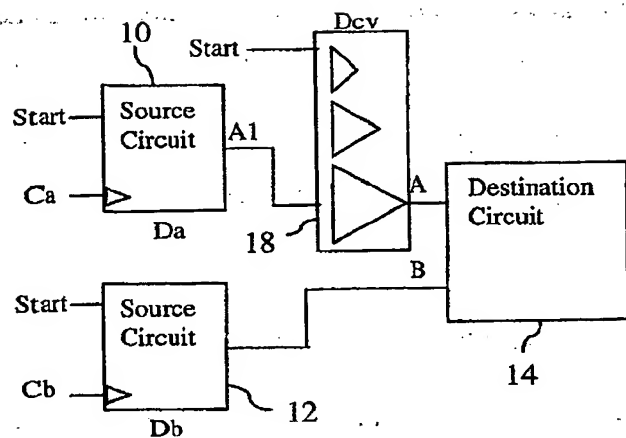


Fig. 3a

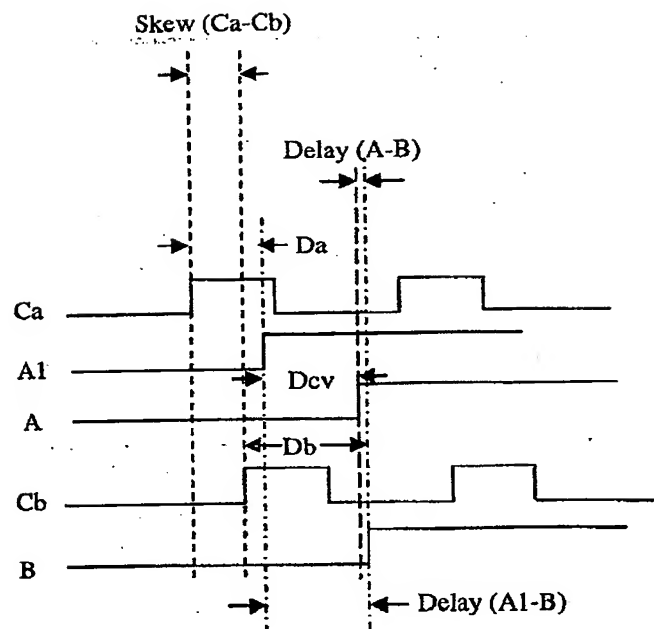


Fig. 3b

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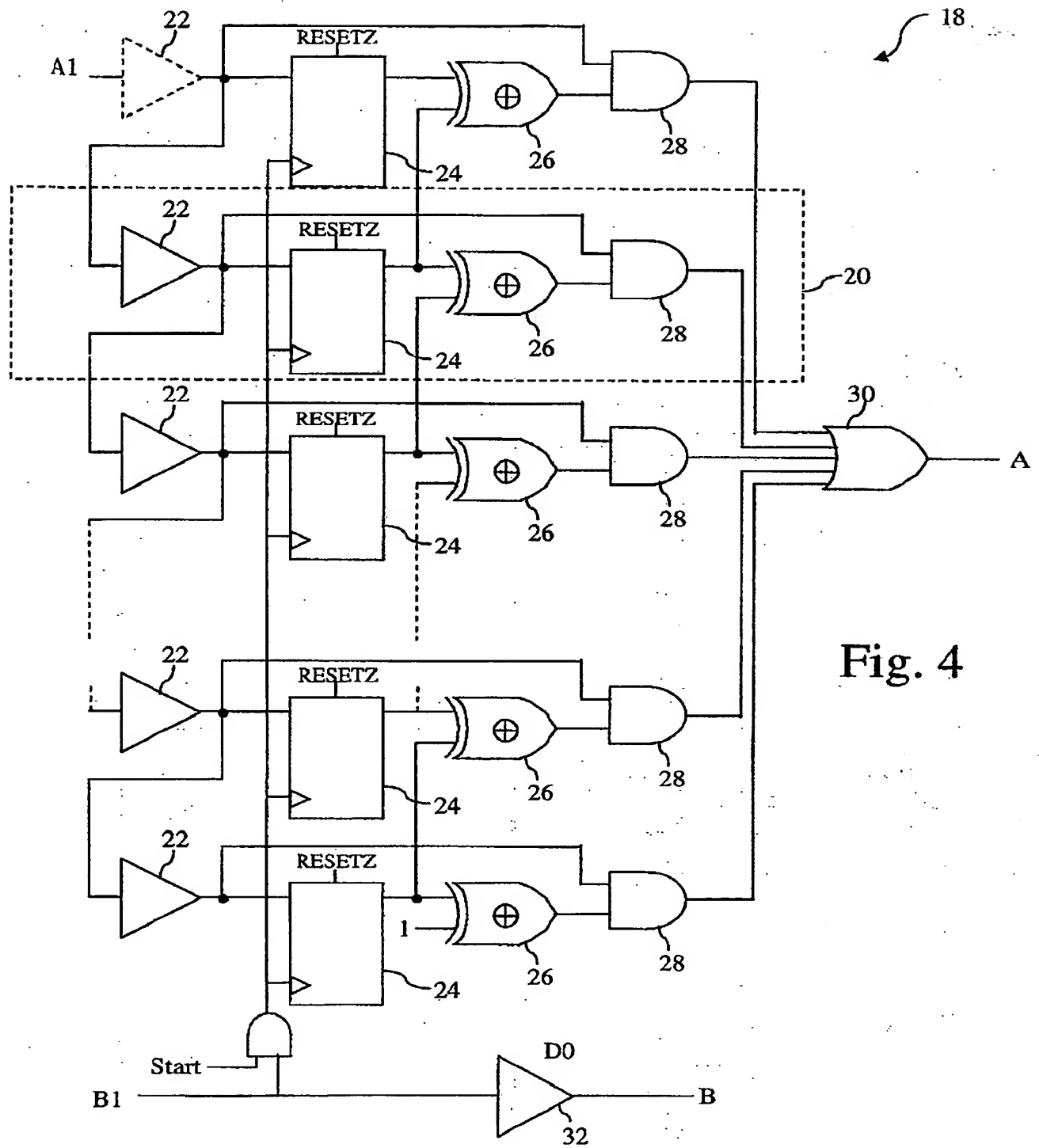


Fig. 4

